METHOD FOR PRODUCING HEAVILY DOPED SEMICONDUCTOR COMPONENTS

Background Information

The present invention is based on a method for producing semiconductor components according to the species defined in the independent claim. When manufacturing semiconductor components, it is known to produce doped regions in a semiconductor wafer with the aid of ion implantation, gas-phase coating (for example, with diborane or POC13), film diffusion or using liquid solutions.

Summary of the Invention

In contrast, the method of the present invention having the features of the independent claim has the advantage that doped regions with very good homogeneity can be produced. To be regarded as a further advantage is that it is possible, both on the front side and on the back side of the semiconductor wafer, to introduce such homogeneous regions even of different doping types in only one diffusion step. It is also possible to provide different levels of dopant concentration on the front side and back side. The heating of the wafer, and with it, the driving of the doping atoms into the interior of the wafer for producing doped regions at high temperatures in the range of about 1200 to 1280 degrees Celsius advantageously ensures a deep and concentrated penetration of the doping atoms into the wafer.

The measures specified in the dependent claims permit advantageous further developments and improvements of the method indicated in the independent claim.

It is particularly advantageous to coat the wafer surfaces with doping atoms using a chemical vapor deposition method, particularly a chemical vapor deposition method at atmospheric pressure (APCVD, "Atmospheric Pressure Chemical Vapor Deposition").

It is thereby possible to achieve extremely high dopant concentrations which reach up to the solubility limit of the silicon wafer.

It is also particularly advantageous to heat the wafer, covered with a glass layer, in oxidizing atmosphere. This advantageously allows the dopant to diffuse into the interior of the wafer in acceptable periods of time.

Furthermore, it is advantageous to cover the glass layer, provided with dopant, with a neutral glass layer prior to the diffusion process. A mutual influencing of the doping of the front side and back side, or of different wafers set up in the diffusion oven at the same time, is thereby reliably prevented.

Brief Description of the Drawing

Exemplary embodiments of the present invention are shown in the Drawing and are explained in detail in the following description. Figure 1 shows a wafer with applied glass layer; Figure 2 shows a wafer after a diffusion process; and Figure 3 shows a wafer after removing the glass layer.

Description of the Exemplary Embodiments

Figure 1 shows a side view of a wire-sawed raw wafer 1 having great surface roughness, upon whose front side a p-doped glass layer 2 is applied, and upon whose back side an n-doped glass layer 4 is applied. Doped glass layers 2 and 4 are covered with a neutral glass layer 3 and 5, respectively.

Glass layers 2 and 4 are used for coating the wafer with dopants. In detail, the production proceeds in the following steps: Raw wafer 1 is first of all heated to about 380 degrees Celsius. This is carried out in that the wafer, in turn with further wafers, is brought on a conveyor belt into a heating chamber provided with gas injectors. The glass layer is subsequently deposited in an APCVD process (APCVD = "Atmospheric Pressure Chemical Vapor Deposition"), thus, a chemical vapor deposition process under atmospheric pressure. In so doing, for example, first of all the front side of the

wafer is exposed to a silane gas, in that gas from the gas injectors to be passed on the conveyor belt flows onto the surface of the wafer. In the case of the front side, B2H6 is admixed to the silane gas. The silane decomposes on the wafer surface heated to 380 degrees Celsius and reacts with oxygen to form silicon dioxide. Because of the B2H6 admixture, this glass is laced with a p-type dopant. Glass layer 2 is grown to a layer thickness of about 2 micrometers. The admixture of the B2H6 gas has been selected in such a way that the glass layer has a boron constituent of about 6 percentage by weight. The glass layer is subsequently exposed to the same silane gas, however, without the addition of B2H6. Neutral glass layer 3 thereby grows on glass layer 2. The process is ended when neutral glass layer 3 has a thickness of about 0.5 micrometers. In a further step, the wafer is turned over and correspondingly coated on the back side with an n-doped glass layer 4 (thickness 2 micrometers, phosphorus constituent of about 6 percentage by weight). The n-doping is achieved by admixing PH3 to the silane gas instead of B2H6. Subsequently, analogous to the front side, a neutral glass layer 5 having a thickness of 0.5 micrometers is applied.

As an alternative to the silane gas method described, the so-called TEOS method (TEOS = tetra-ethyl-ortho-silicate) can be used, which can likewise proceed under normal pressure. In this case, instead of silane gas, $Si(OC_2H_5)_4$ gas is used, the tetraethyl orthosilicate depositing on the wafer surface decomposing on the surface heated to 380 degrees Celsius and reacting with oxygen to form silicon dioxide. In this case, the doping is effected by gas admixture of trimethyl phosphate or trimethyl borate.

Figure 2 shows the wafer after a diffusion process, having a heavily p-doped region 10 and a heavily n-doped region 11.

The diffusion process, carried out after the coating with doped glass layers, takes place in a diffusion oven at a temperature of 1200 to 1280 degrees Celsius, preferably at a temperature of about 1265 degrees Celsius. A plurality of wafers to be processed simultaneously are arranged upright in a setup made of silicon carbide or polysilicon and having retaining elements. This heating is maintained approximately 20 to 30 hours, preferably 21 hours, and in particular is carried out in oxidizing atmosphere.

With a diffusion time of 21 hours for driving the dopants, stored on the surface in the form of glass layers, into the interior of the wafer, phosphorus and boron dosages, respectively, of about 1-2 x 10^{17} cm^{-2} are achieved in regions 10 and 11. This is a dosage higher by an order of magnitude than for semiconductor applications otherwise typical.

In alternative specific embodiments of the diffusion step, it is also possible to stack wafers to be processed simultaneously, direct mutual contact of the wafers being prevented by sprinkling with aluminum oxide powder beforehand, or by interposing neutral films, known from film diffusion.

In a further step, using, for example, 50 percentage hydrofluoric acid, applied glass layers 2, 3, 4 and 5 are removed again, resulting in wafer 1 shown in Figure 3 that is doped on both sides with a heavily p-doped region 10 on the front side and a heavily n-doped region 11 on the back side. This wafer can now be used, for instance, for producing high-blocking-capability p-n diodes (two-layer diodes) by applying metal contactings on both sides in further steps. To produce the metal contactings, for example, metal layers are deposited by sputtering simultaneously on both sides of the wafer, first of all a chromium layer 70 nanometers thick, followed by a nickel-vanadium layer 160 nanometers thick and a silver layer 100 nanometers thick. The wafer is subsequently divided along dividing lines into individual diode chips, the dividing lines having optionally already been introduced into the wafer by sawing prior to applying the metal contactings.

The method of the present invention is suitable not only for two-layer diodes, but can also be utilized in appropriately modified form for producing multi-layered diodes, particularly diode thyristors (four-layer diodes) and three-layer diodes (transistor diodes). Power semiconductors, e.g. power diodes, in particular can be easily and reliably produced by the high doping dosages attainable. Thyristors and bipolar transistors can also be produced with the method.